AMENDMENTS TO THE CLAIMS

1. (Canceled)

2. (Original) A method of reading a plurality of N data bits of a data burst comprising:

storing said N data bits at respective memory locations in burst order such that a preceding data bits of said burst is electrically closer to a multiplexer than a next subsequent data bit of said burst;

transferring said N data bits to said multiplexer; and,

outputting said N data bits from said multiplexer in burst order.

3. (Original) A method of storing a plurality of data bits comprising:

receiving first and second data bit values at first and second memory locations respectively;

transferring said first and second data bit values to first and second multiplexer locations respectively;

completing said transfer of said first bit value from said multiplexer prior to completing said transfer of said second bit value; and

outputting said first bit value from said multiplexer prior to completing transfer of said second bit value.

4. (Original) A method of recovering data from a data quadrant of a memory integrated circuit comprising:

receiving a data address from an external address source;

concurrently reading a plurality of bits of data from a respective plurality of memory locations, said locations selected according to said address;

storing said respective plurality of bits in a respective plurality of multiplexer input locations;

outputting said respective plurality of bits from said respective multiplexer input locations in a particular time sequence such that a first bit output is a bit retrieved from one of said plurality of memory locations electrically closest to said respective buffer location.

Claims 5-7 (Cancelled)

8. (Original) A memory integrated circuit device comprising:

a multiplexer including a plurality of inputs for receiving data, said multiplexer adapted to output data in a particular chronological order such that data received at a first one of said plurality of inputs is output before data received at a last one of said plurality of inputs;

a plurality of memory cells disposed at a respective plurality of different locations; and

a plurality of connecting paths, each paths of said plurality having a characteristic electrical length, each said path switchingly connected between one of said plurality of cells and one of said plurality of multiplexer inputs, the path of said plurality having a shortest electrical length being switchingly connected to said first multiplexer input.

9. (Original) A device as in claim 8 further comprising:

an address decoder having an address input adapted to receiving a plurality of encoded address signals;

said address decoder having a plurality of outputs each operatively connected to, and adapted to select, a particular plurality of said cells;

said address decoder adapted to uniquely activate one of said plurality of outputs in response to a unique address signal identifying said plurality.

10. (Original) A device as in claim 8 wherein each said connecting path includes traces and devices.

Claims 11-13 (Cancelled)

14. (Original) A memory integrated circuit device comprising:

an address decoder circuit;

a memory bank including a first plurality of memory bit storage locations;

a multiplexer including a second plurality of demux bit storage locations, said plurality of demux bit storage locations arranged according to a particular output order, said output order including a first output bit;

a plurality of electrical connections, each including a sense amplifier and a conductive trace, each of said plurality of electrical connections operatively connecting a memory bit storage location of said first plurality to a respective demux storage location of said second plurality, each of said plurality of electrical connections having a characteristic electrical length; and

an electrical connection of said plurality of electrically connections operatively connected to said first output bit having a characteristic electrical length no longer than the characteristic electrical length of any other electrical connection of said plurality of electrical connections.

Claims 15-16 (Cancelled)

17. (Original) A serial data output signal comprising:

a plurality of data bits forming a data burst, said plurality of data bits including a first-output data bit and a last-output data bit, said first-output data bit representing a value stored in a first memory cell and said last-output data bit representing a value stored in a second memory cell, said first and second memory cells incorporated in a memory device including a multiplexer and located at respective first and second electrical distances from said multiplexer, said first electrical distance being shorter than said second electrical distance.

18. (Original) A serial data output signal as a claim 17 wherein said first bit is output from said multiplexer at a time prior to the arrival of said second bit at said multiplexer, both bits being output during a single read cycle of said memory device.

19. (Original) A computer processing system comprising:

a central processing unit;

a digital memory operatively connected to said central processing unit by means of a communication bus, said digital memory including an address decoder, a multiplexer, and first and second memory cells at respective first and second electrical distances from said multiplexer, said first electrical distance being shorter than said second electrical distance, said first and second memory cells adapted to store first and second data values respectively, said buffer adapted to receive respective first and second signals corresponding to said first and second data values from said first and second memory cells respectively and to output said first signal to said central processing unit before outputting said second signal, thereby adhering to a fixed burst order.